# B.Sc. (Data Science)
# Core Course (CC)
# Semester IV
# BSDB32401T: Computer System Architecture

**Total Marks: 100**
**External Marks: 70**
**Internal Marks: 30**
**Credits: 4**
**Pass Percentage: 40%**

**Objective**
This course will illustrate various elementary concepts of Digital Electronics including Number System, Boolean algebra and Combinational Circuits and comprehend the design of basic computer using instruction formats, addressing modes and various memory management techniques and algorithms.

**INSTRUCTIONS FOR THE PAPER SETTER/EXAMINER**
1. The syllabus prescribed should be strictly adhered to.
2. The question paper will consist of three sections: A, B, and C. Sections A and B will have four questions from the respective sections of the syllabus and will carry 10 marks each. The candidates will attempt two questions from each section.
3. Section C will have fifteen short answer questions covering the entire syllabus. Each question will carry 3 marks. Candidates will attempt any ten questions from this section.
4. The examiner shall give a clear instruction to the candidates to attempt questions only at one place and only once. Second or subsequent attempts, unless the earlier ones have been crossed out, shall not be evaluated.
5. The duration of each paper will be three hours.

**INSTRUCTIONS FOR THE CANDIDATES:**
Candidates are required to attempt any two questions each from the sections A and B of the question paper and any ten short questions from Section C. They have to attempt questions only at one place and only once. Second or subsequent attempts, unless the earlier ones have been crossed out, shall not be evaluated.

**Section A**

**Unit I: Basics of Data Representation-** Number System, Conversions of Number Systems, 1's and 2's Complements, fixed and floating point representation, character representation, addition, subtraction, magnitude comparison.

**Unit II**: **Introduction to Boolean algebra** - Logic gates, Boolean algebra, K-Maps, Sum of Products, Product of Sums.

**Unit III: Combinational circuits and Sequential Circuits:** decoders, multiplexors, Encoders, DE-multiplexers Half Adders, Full Adders, Flip Flops, registers, counters and memory units.

**Unit IV: Basic Computer Organization and Design**- Computer Architecture, Structure, Computer registers, Common Bus Systems, Arithmetic, Logical, Shift Microperations, and Design of ALU.

**Section B**

**Unit V: Timing and Control Unit**-Instruction cycle, Memory reference instructions, Register reference instructions, Input-output instructions, Design of Timing and Control Unit.

**Unit VI: Design of Central Processing Unit:** Register organization, stack organization, Register Organization, one address instructions, two address instructions, and three address instructions. Instruction formats, addressing modes.

**Unit VII: Input-Output Organization:** I/O interfaces, Data transfer schemes. I/O control mechanisms - Program controlled, Interrupt controlled and DMA controller.

**Unit VIII**: **Memory Unit**: Memory hierarchy, High-speed memories, Organization of a Cache memory unit, Virtual memory, Memory management.

**Suggested Readings**

1. Mano, Morris M., Computer System Architecture, 3rd ed.,Prentice Hall, 2007
2. Hayes, J.P., Computer Architecture and Organization, McGraw Hill, 1998
3. Hennessy, J.L., Patterson, D.A, and Goldberg, D., Computer Architecture A Quantitative
4. Approach, Pearson Education Asia, 2005
5. Leigh, W.E. and Ali, D.L., System Architecture: software and hardware concepts, South Wester Publishing Co., 2000